AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of the claims.

Listing of the Claims:

1.-6. (Canceled)

7. (Currently amended) A method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising:

~~forming a device isolation structure in a semiconductor substrate including the cell region and the peripheral circuit region;~~

forming a tunnel oxide layer and a floating gate layer ~~over the cell region~~ on a semiconductor substrate including a cell region and a peripheral region;

removing the floating gate layer and the tunnel oxide layer formed on the peripheral region;

forming a dielectric layer and a control gate layer ~~over the floating gate layer of~~ on the cell region and ~~on the semiconductor substrate of~~ the peripheral circuit region of the semiconductor substrate, the dielectric layer including an oxide layer and a nitride layer; and

forming a source and a drain region in the semiconductor substrate by performing an impurity ion implantation process.

8. (Previously presented) The method of manufacturing the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, wherein the dielectric layer is formed by stacking at least two or more layers of at least one of the oxide layer and the nitride layer.

9. (Currently Amended) The method of manufacturing the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, wherein the dielectric layer is formed in thickness of about 30~300[[□]]Å.

10. (Previously presented) The method of manufacturing the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, wherein the dielectric layer is formed by stacking a first oxide layer, a nitride layer and a second oxide layer.

11. (Previously presented) The method of manufacturing the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, wherein the dielectric layer is formed by stacking a first oxide layer, a first nitride layer, a second oxide layer and a second nitride layer.

12. (Previously presented) The method of manufacturing the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, wherein the dielectric layer is formed by stacking a first oxide layer, a first nitride layer, a second oxide layer, a second nitride layer and a third oxide layer.

13. (Currently amended) A method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising:

~~forming a device isolation structure in a semiconductor substrate including the cell region and the peripheral circuit region;~~

forming a tunnel oxide layer and a floating gate layer ~~over the cell region~~ on a semiconductor substrate including a cell region and a peripheral region;

removing the floating gate layer and the tunnel oxide layer formed on the peripheral region;

forming a dielectric layer and a control gate layer ~~over the floating gate of~~ on the cell region and ~~on the semiconductor substrate of~~ the peripheral region of the semiconductor substrate, the dielectric layer including a first oxide layer, a first nitride layer, a second oxide layer, a second nitride layer and a third oxide layer; and

forming a source and a drain region in the semiconductor substrate by performing an impurity ion implantation process.

14. (Previously presented) The method of manufacturing the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 7, the floating gate layer and the control gate layer is formed of polysilicon.

15. (Previously presented) The method of manufacturing the code address memory cell in the peripheral region and the flash memory cell in the cell region according to claim 13, the floating gate layer and the control gate layer is formed of polysilicon.